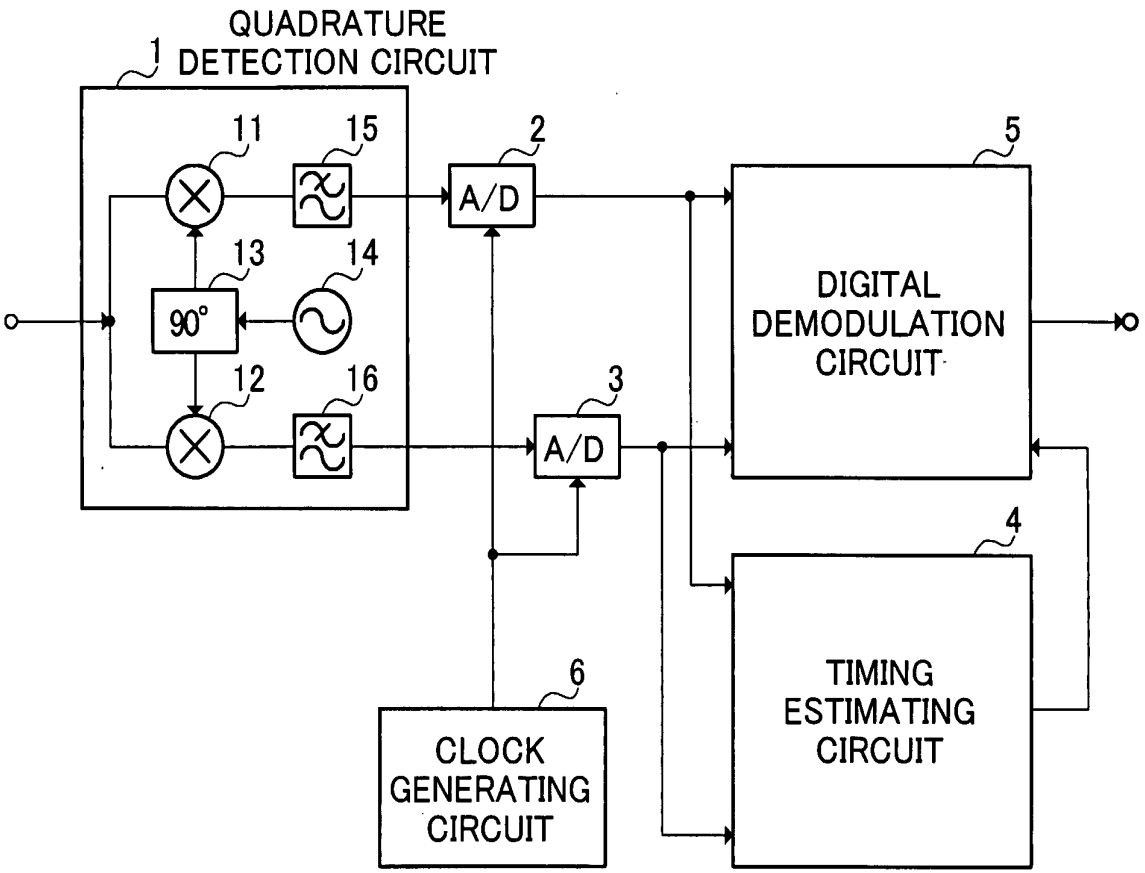

PRIOR ART

FIG.1

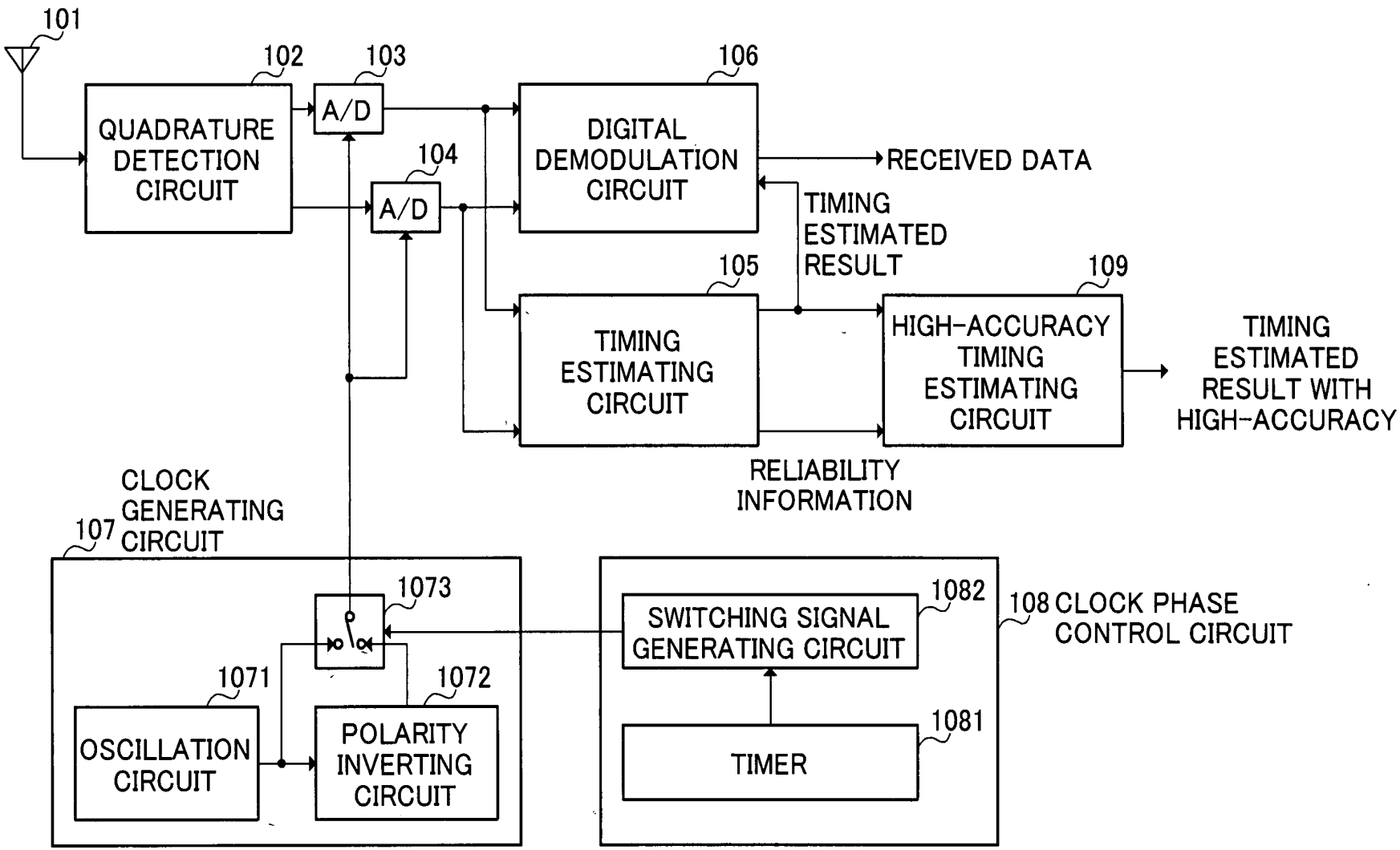
101
102
103
106
QUADRATURE DETECTION CIRCUIT
A/D
DIGITAL DEMODULATION CIRCUIT
RECEIVED DATA
104
A/D
TIMING ESTIMATED RESULT
105
109
TIMING ESTIMATING CIRCUIT
HIGH-ACCURACY TIMING ESTIMATING CIRCUIT
TIMING ESTIMATED RESULT WITH HIGH-ACCURACY
RELIABILITY INFORMATION
CLOCK GENERATING CIRCUIT
107
1073
1082
SWITCHING SIGNAL GENERATING CIRCUIT
108 CLOCK PHASE CONTROL CIRCUIT
1071
1072
OSCILLATION CIRCUIT
POLARITY INVERTING CIRCUIT
1081
TIMER

FIG.2

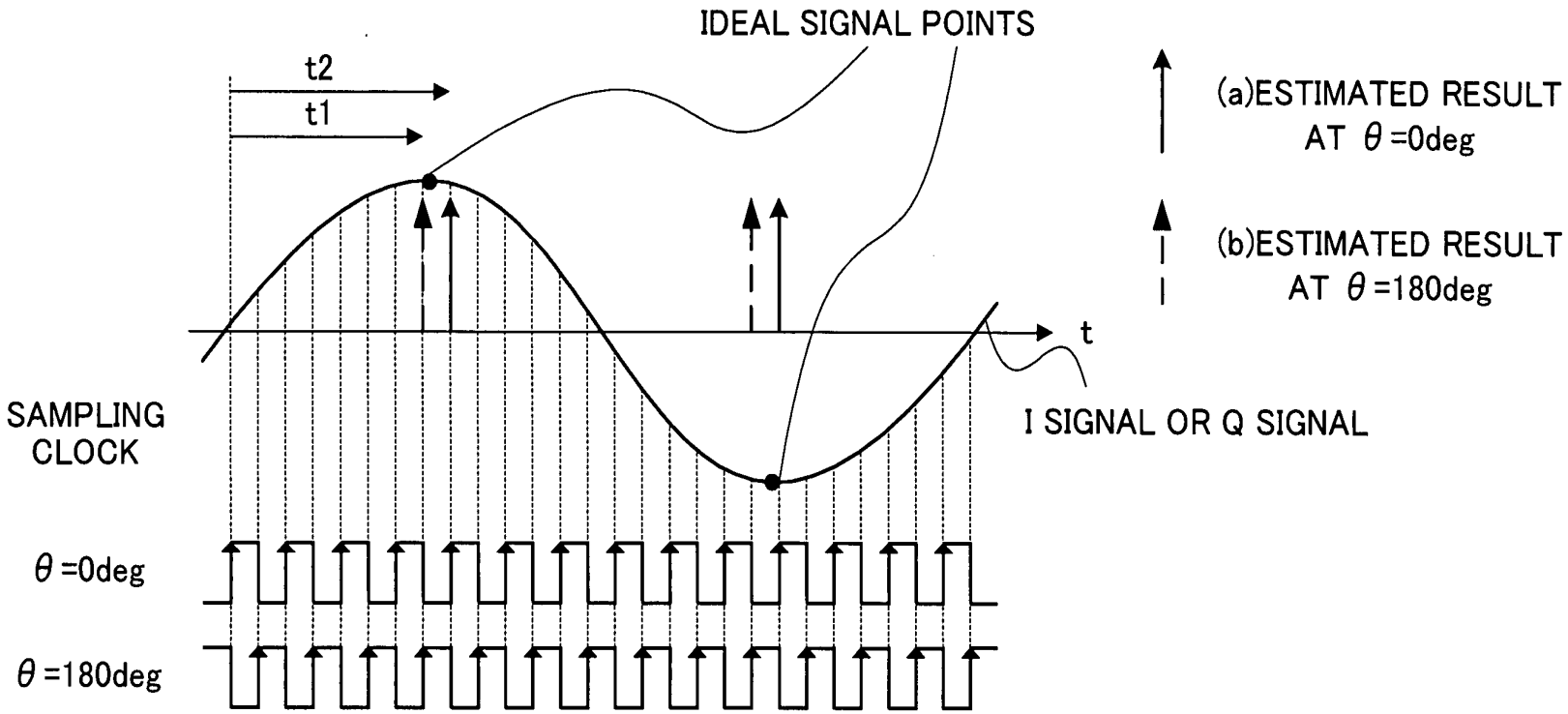
IDEAL SIGNAL POINTS
t2
t1
(a)ESTIMATED RESULT
AT θ =0deg
(b)ESTIMATED RESULT
AT θ =180deg
t
I SIGNAL OR Q SIGNAL
SAMPLING
CLOCK
θ =0deg
θ =180deg

FIG.3

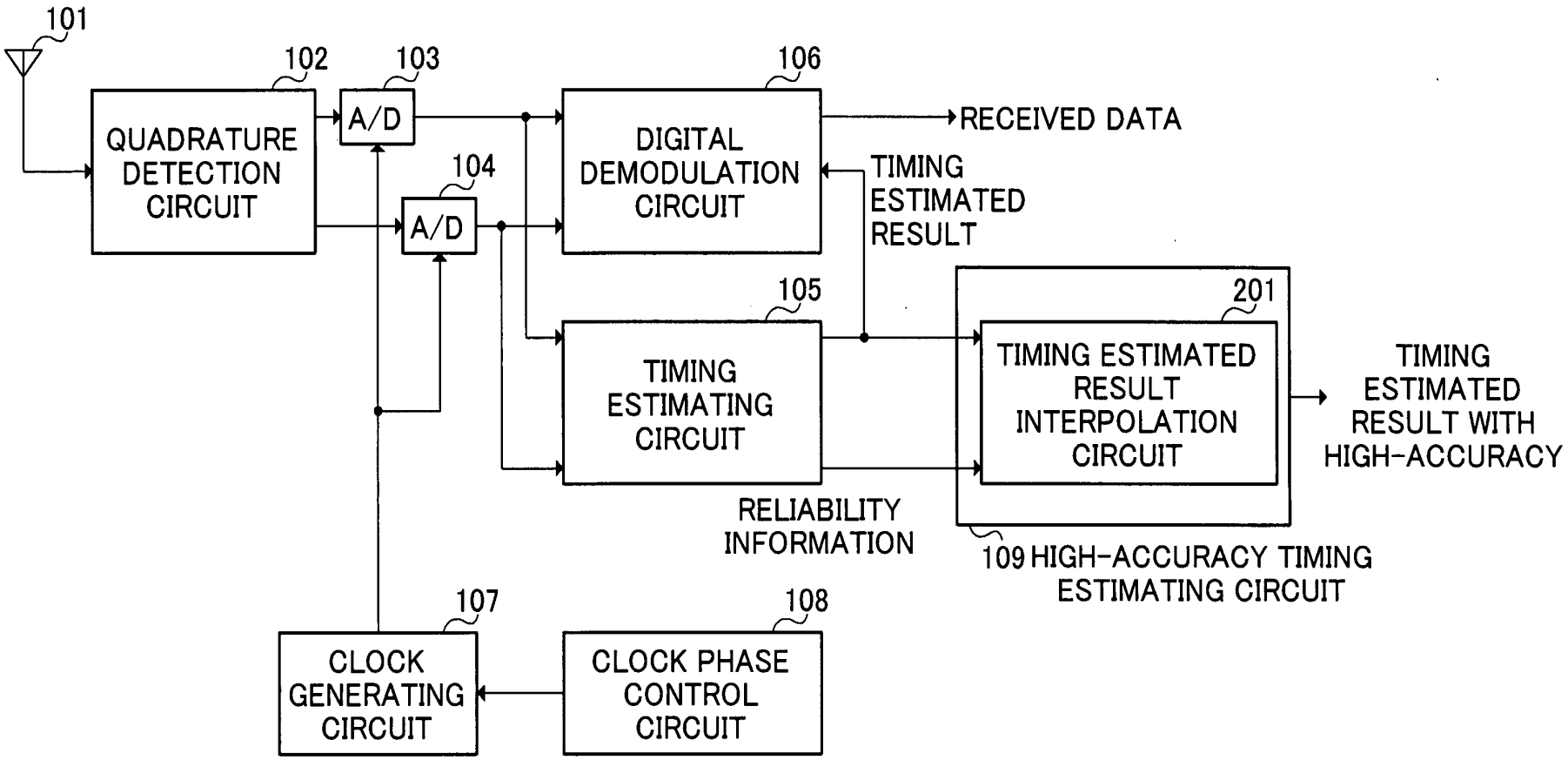
101
102
103
106
QUADRATURE DETECTION CIRCUIT
A/D
DIGITAL DEMODULATION CIRCUIT
RECEIVED DATA
104
A/D
TIMING ESTIMATED RESULT
105
201
TIMING ESTIMATING CIRCUIT
TIMING ESTIMATED RESULT INTERPOLATION CIRCUIT
TIMING ESTIMATED RESULT WITH HIGH-ACCURACY
RELIABILITY INFORMATION
109 HIGH-ACCURACY TIMING ESTIMATING CIRCUIT
107
108
CLOCK GENERATING CIRCUIT
CLOCK PHASE CONTROL CIRCUIT

FIG.4

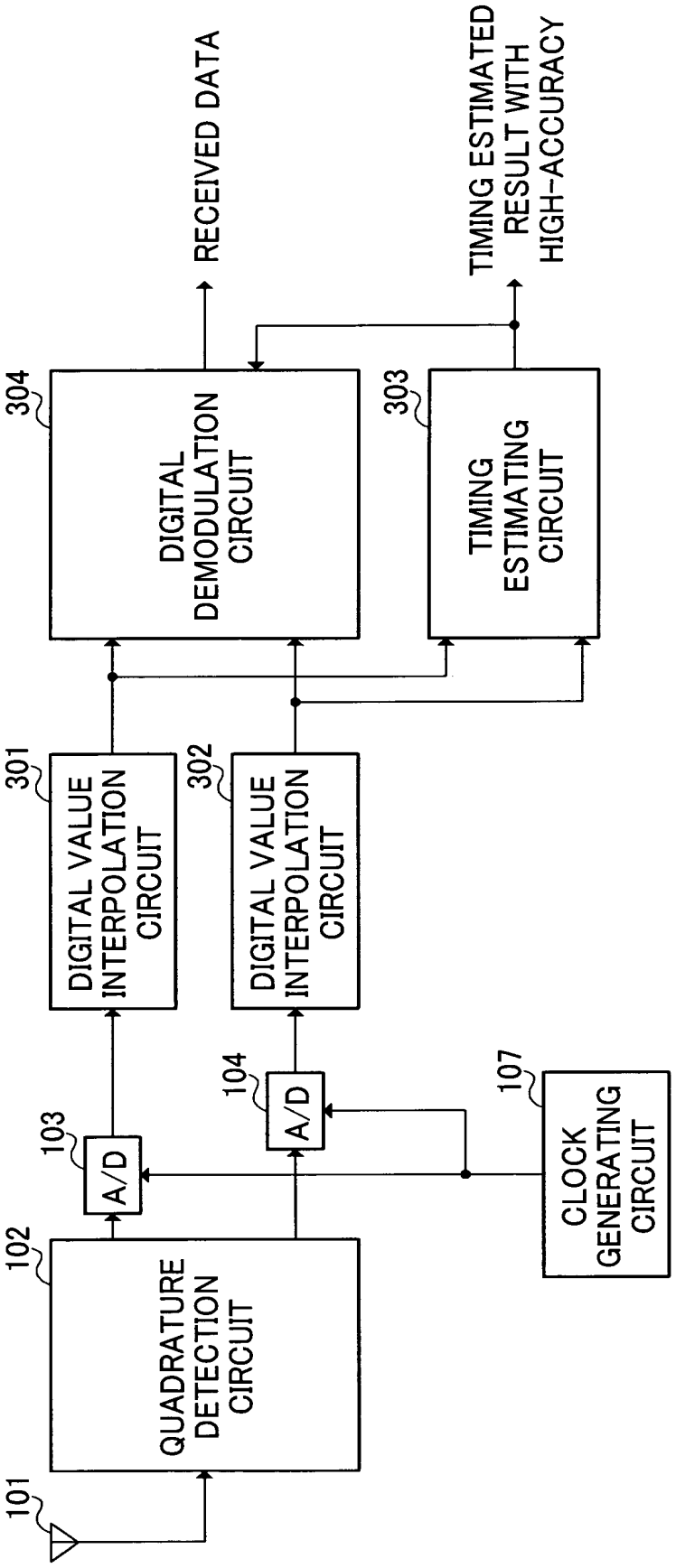
101
QUADRATURE DETECTION CIRCUIT
102
A/D
103
A/D
104
CLOCK GENERATING CIRCUIT
107
DIGITAL VALUE INTERPOLATION CIRCUIT
301
DIGITAL VALUE INTERPOLATION CIRCUIT
302
DIGITAL DEMODULATION CIRCUIT
304
TIMING ESTIMATING CIRCUIT
303
RECEIVED DATA
TIMING ESTIMATED RESULT WITH HIGH-ACCURACY

FIG.5

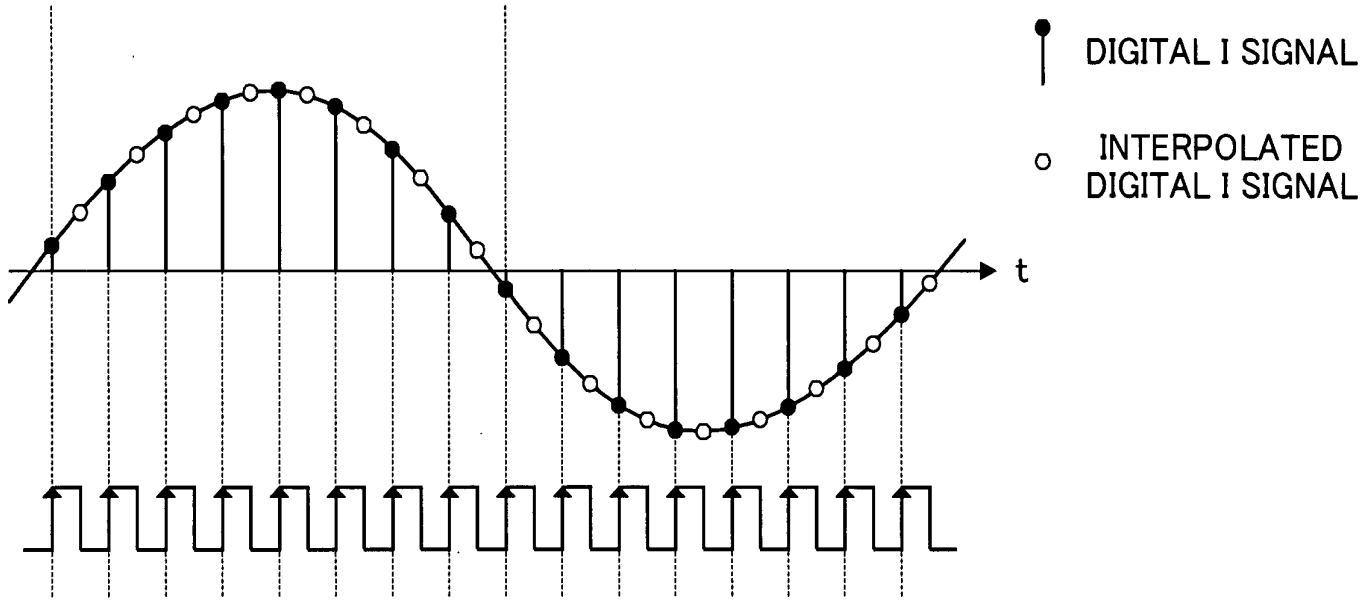

FIG.6

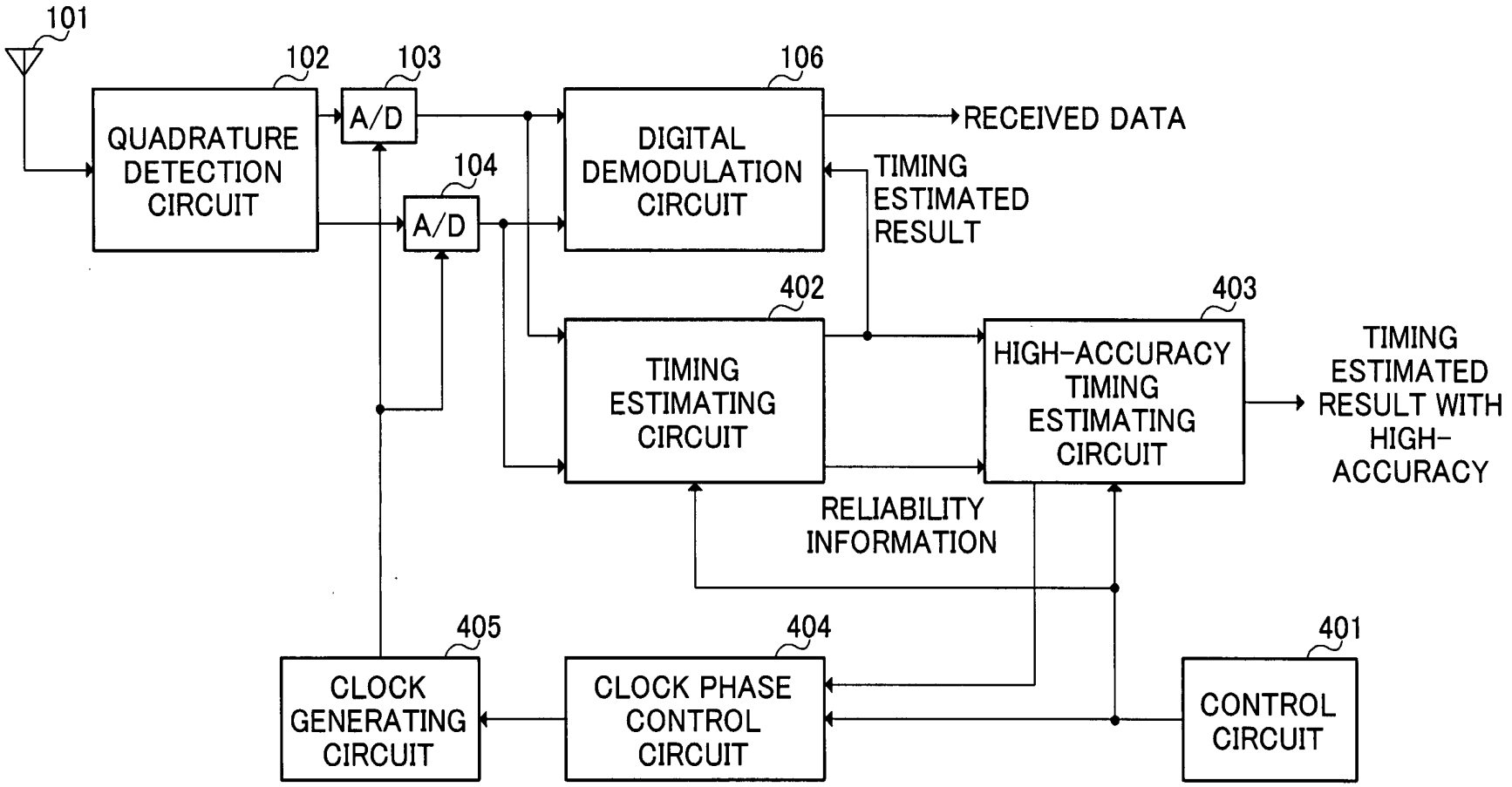
101
102
103
106
QUADRATURE DETECTION CIRCUIT
A/D
DIGITAL DEMODULATION CIRCUIT
RECEIVED DATA
104
A/D
TIMING ESTIMATED RESULT
402
403
TIMING ESTIMATING CIRCUIT
HIGH-ACCURACY TIMING ESTIMATING CIRCUIT
TIMING ESTIMATED RESULT WITH HIGH-ACCURACY
RELIABILITY INFORMATION
405
404
401
CLOCK GENERATING CIRCUIT
CLOCK PHASE CONTROL CIRCUIT
CONTROL CIRCUIT

FIG.7

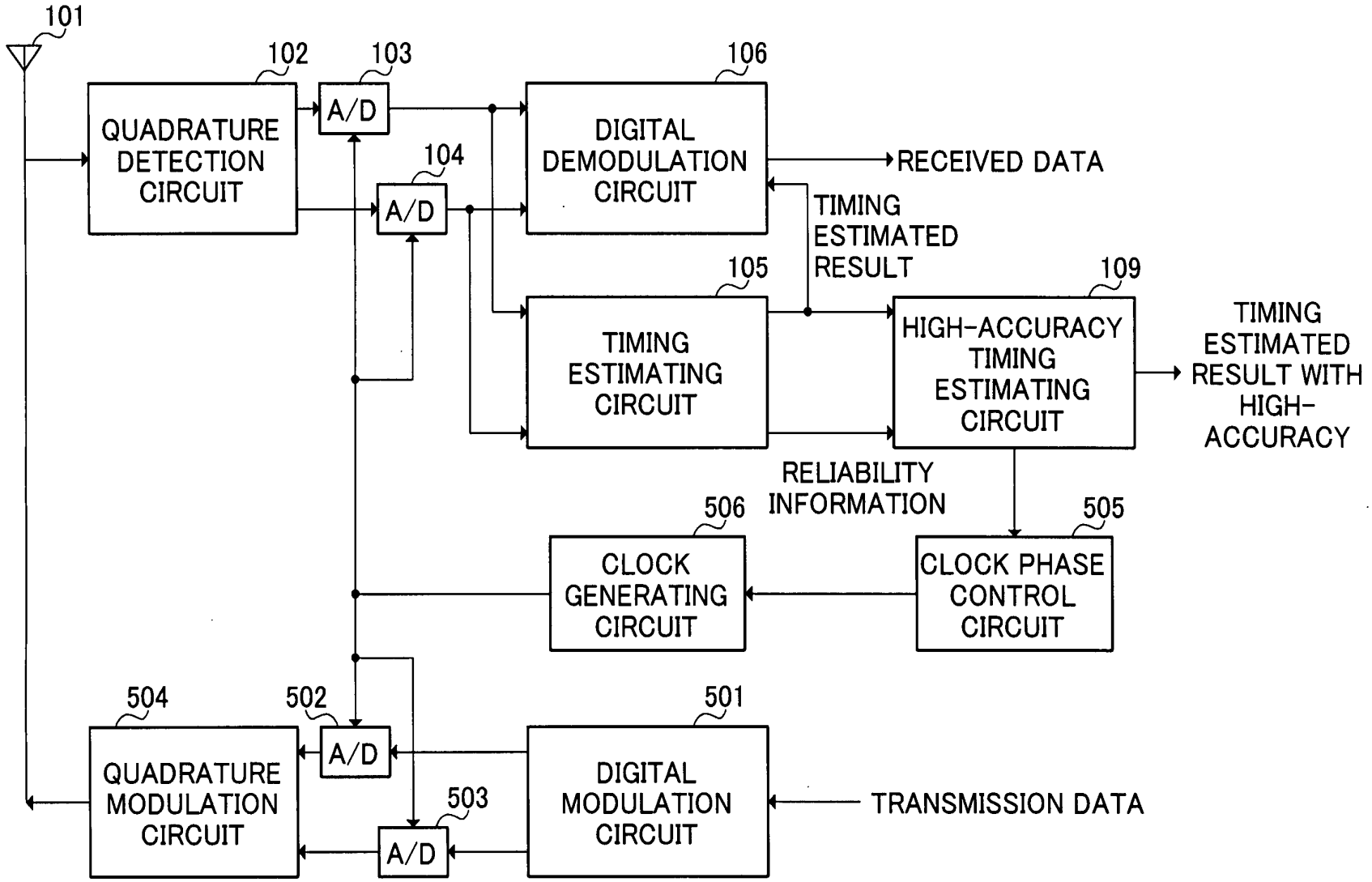
101
102
103
106
QUADRATURE DETECTION CIRCUIT
A/D
DIGITAL DEMODULATION CIRCUIT
RECEIVED DATA
104
A/D
TIMING ESTIMATED RESULT
105
109
TIMING ESTIMATING CIRCUIT
HIGH-ACCURACY TIMING ESTIMATING CIRCUIT
TIMING ESTIMATED RESULT WITH HIGH-ACCURACY
RELIABILITY INFORMATION
506
505
CLOCK GENERATING CIRCUIT
CLOCK PHASE CONTROL CIRCUIT
504
502
501
QUADRATURE MODULATION CIRCUIT
A/D
DIGITAL MODULATION CIRCUIT
TRANSMISSION DATA
503
A/D

FIG.8

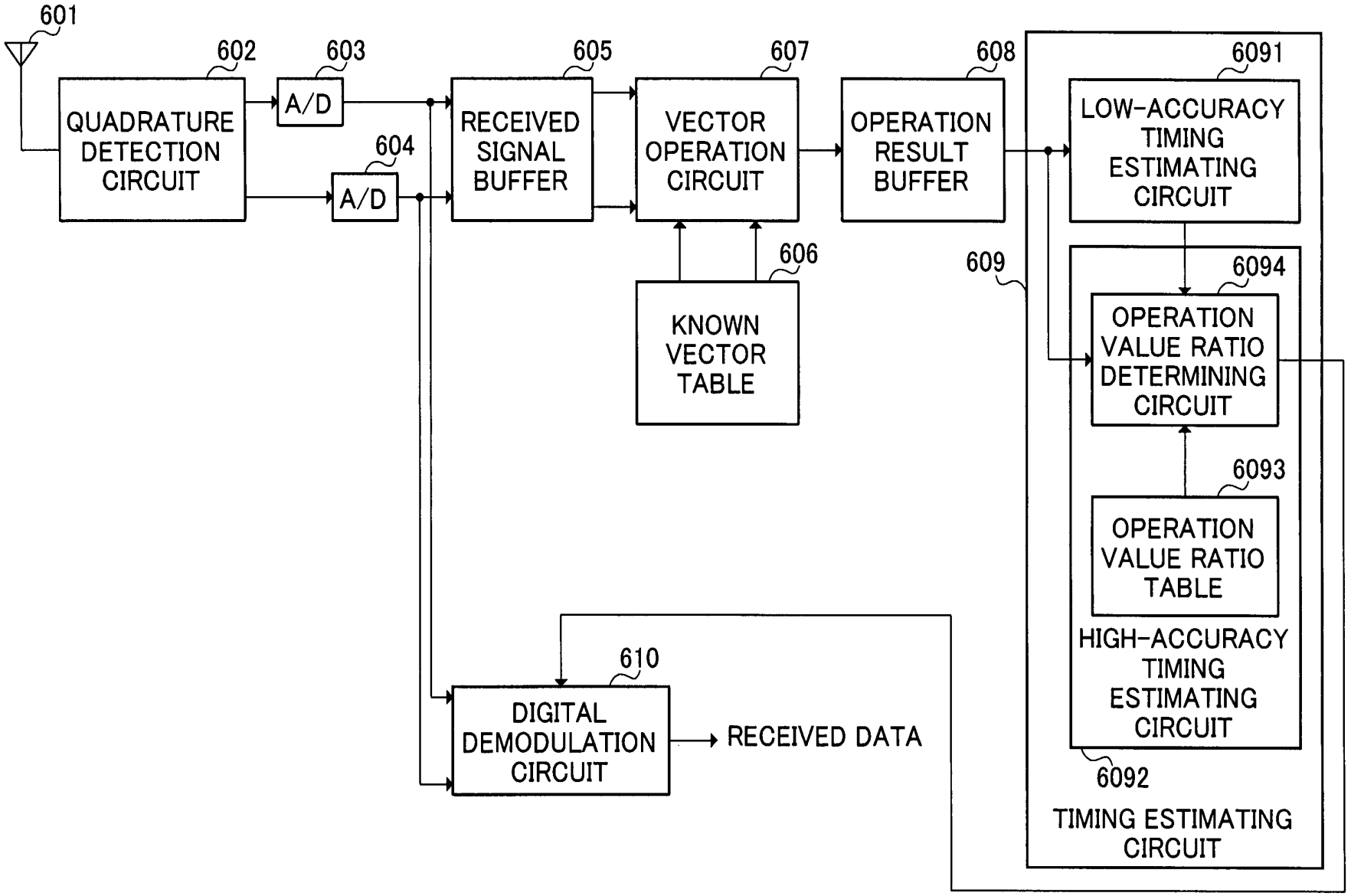
601
602
603
605
607
608
6091
QUADRATURE DETECTION CIRCUIT
A/D
RECEIVED SIGNAL BUFFER
VECTOR OPERATION CIRCUIT
OPERATION RESULT BUFFER
LOW-ACCURACY TIMING ESTIMATING CIRCUIT
604
A/D
606
609
6094
KNOWN VECTOR TABLE
OPERATION VALUE RATIO DETERMINING CIRCUIT
6093
OPERATION VALUE RATIO TABLE
HIGH-ACCURACY TIMING ESTIMATING CIRCUIT
610
DIGITAL DEMODULATION CIRCUIT
RECEIVED DATA
6092
TIMING ESTIMATING CIRCUIT

FIG.9

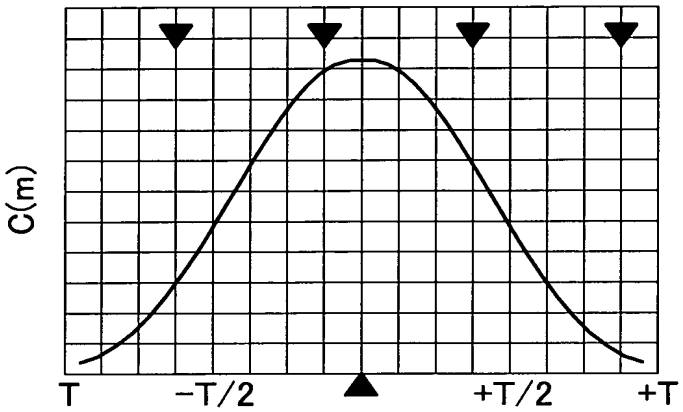

FIG.10A EXAMPLE OF CORRELATION VALUE OBTAINED BY VECTOR OPERATION

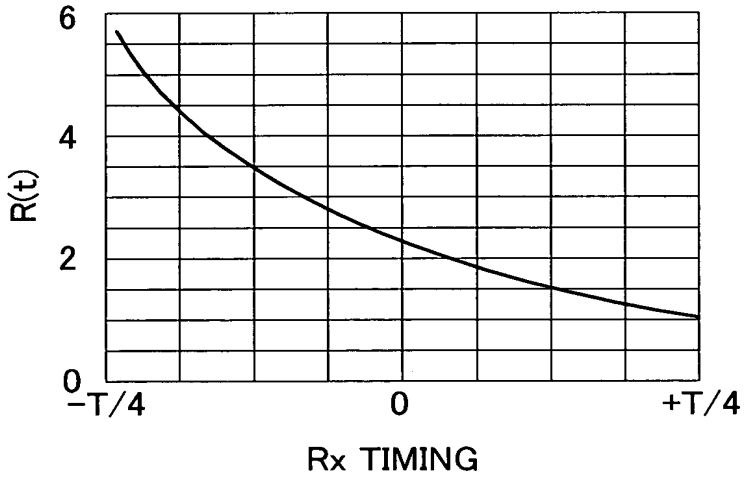

FIG.10B EXAMPLE OF OPERATION VALUE RATIO TABLE VALUE

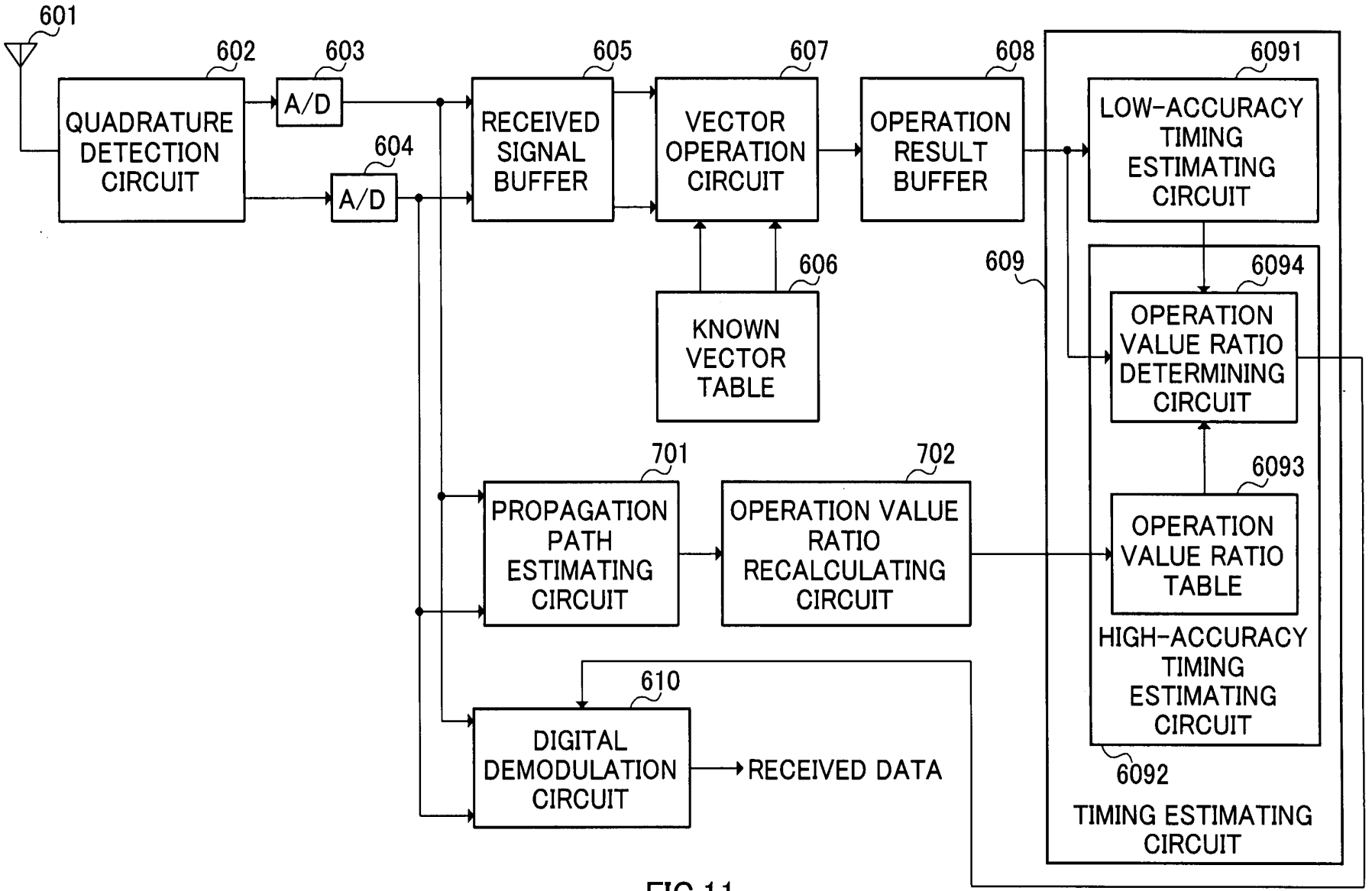
601
602
QUADRATURE DETECTION CIRCUIT
603
A/D
604
A/D
605
RECEIVED SIGNAL BUFFER
607
VECTOR OPERATION CIRCUIT
608
OPERATION RESULT BUFFER
606
KNOWN VECTOR TABLE
609
6091
LOW-ACCURACY TIMING ESTIMATING CIRCUIT
6094
OPERATION VALUE RATIO DETERMINING CIRCUIT
6093
OPERATION VALUE RATIO TABLE
HIGH-ACCURACY TIMING ESTIMATING CIRCUIT
6092
TIMING ESTIMATING CIRCUIT
701
PROPAGATION PATH ESTIMATING CIRCUIT
702
OPERATION VALUE RATIO RECALCULATING CIRCUIT
610
DIGITAL DEMODULATION CIRCUIT
RECEIVED DATA

FIG.11

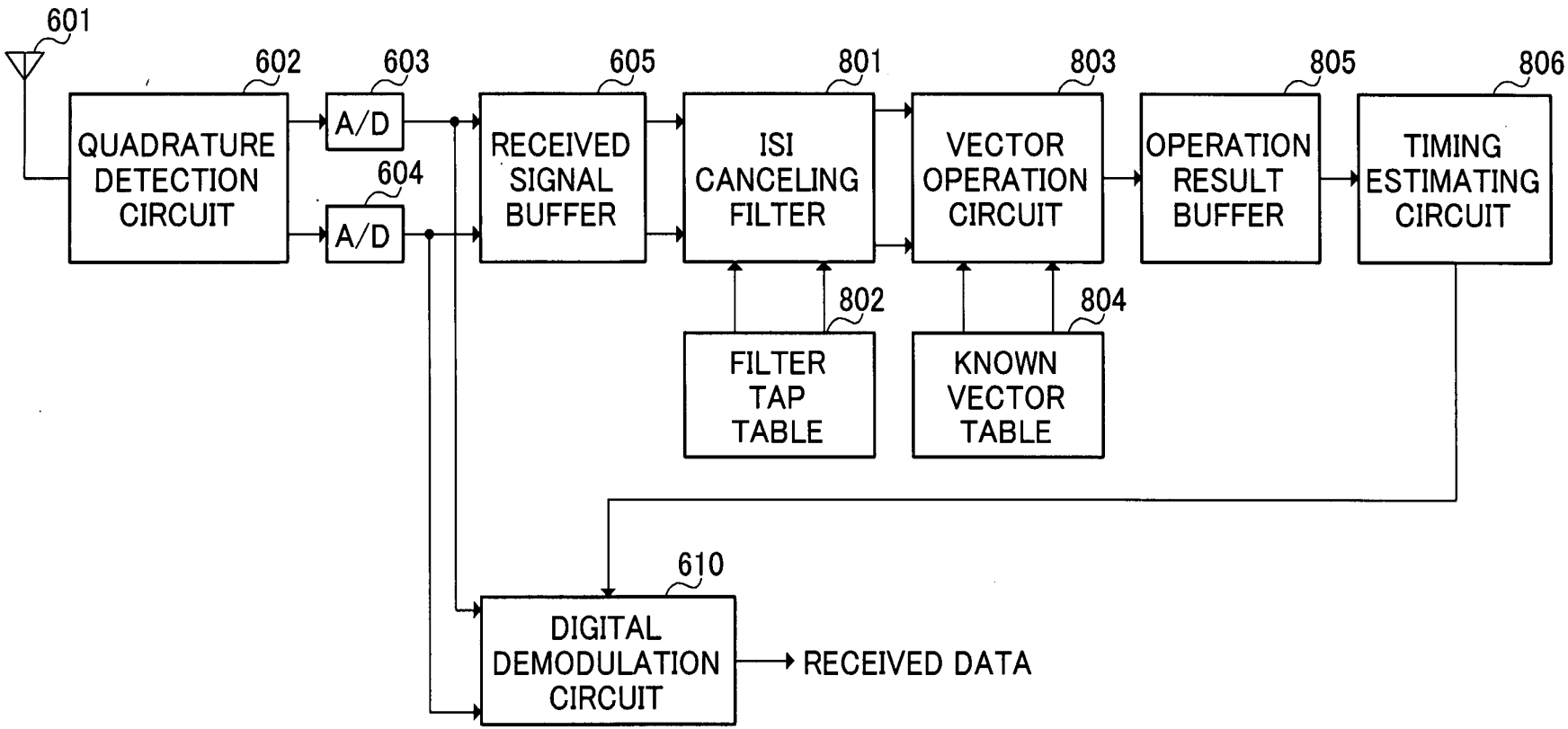
601
602
603
605
801
803
805
806
QUADRATURE DETECTION CIRCUIT
A/D
604
A/D
RECEIVED SIGNAL BUFFER
ISI CANCELING FILTER
VECTOR OPERATION CIRCUIT
OPERATION RESULT BUFFER
TIMING ESTIMATING CIRCUIT
802
804
FILTER TAP TABLE
KNOWN VECTOR TABLE
610
DIGITAL DEMODULATION CIRCUIT
RECEIVED DATA

FIG.12

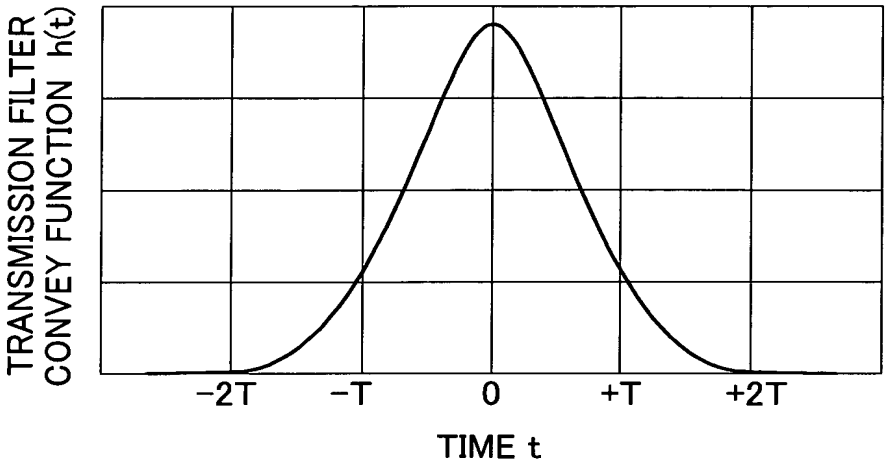

FIG.13A EXAMPLES OF TRANSMISSION BAND-PASS FILTER CARACTERISTICS INCLUDING ISI

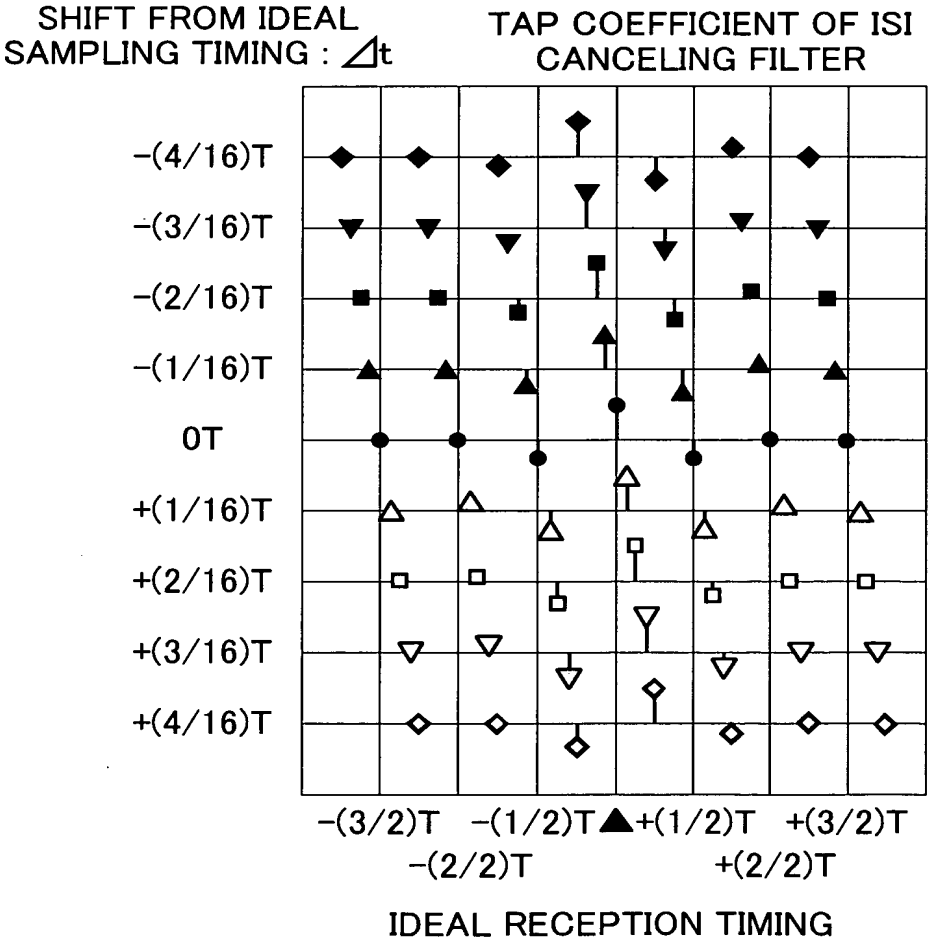

FIG.13B EXAMPLES OF OF ISI CANCELING FILTER TAP COEFFICIENTS FOR SIGNALS SAMPLED AT SHIFTED TIMINGS

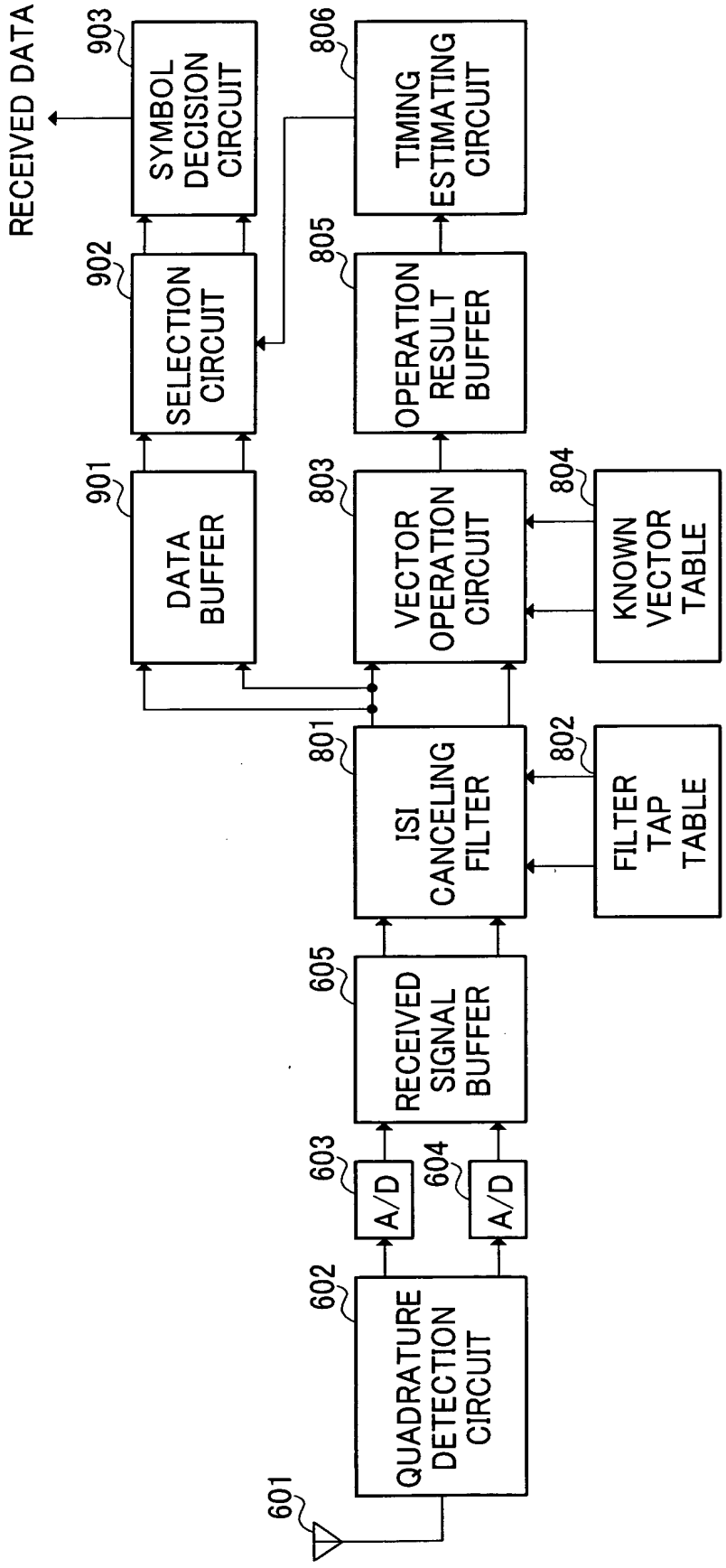
RECEIVED DATA
903
SYMBOL DECISION CIRCUIT
806
TIMING ESTIMATING CIRCUIT
902
SELECTION CIRCUIT
805
OPERATION RESULT BUFFER
901
DATA BUFFER
803
VECTOR OPERATION CIRCUIT
804
KNOWN VECTOR TABLE
801
ISI CANCELING FILTER
802
FILTER TAP TABLE
605
RECEIVED SIGNAL BUFFER
603
A/D
604
A/D
602
QUADRATURE DETECTION CIRCUIT
601

FIG.14

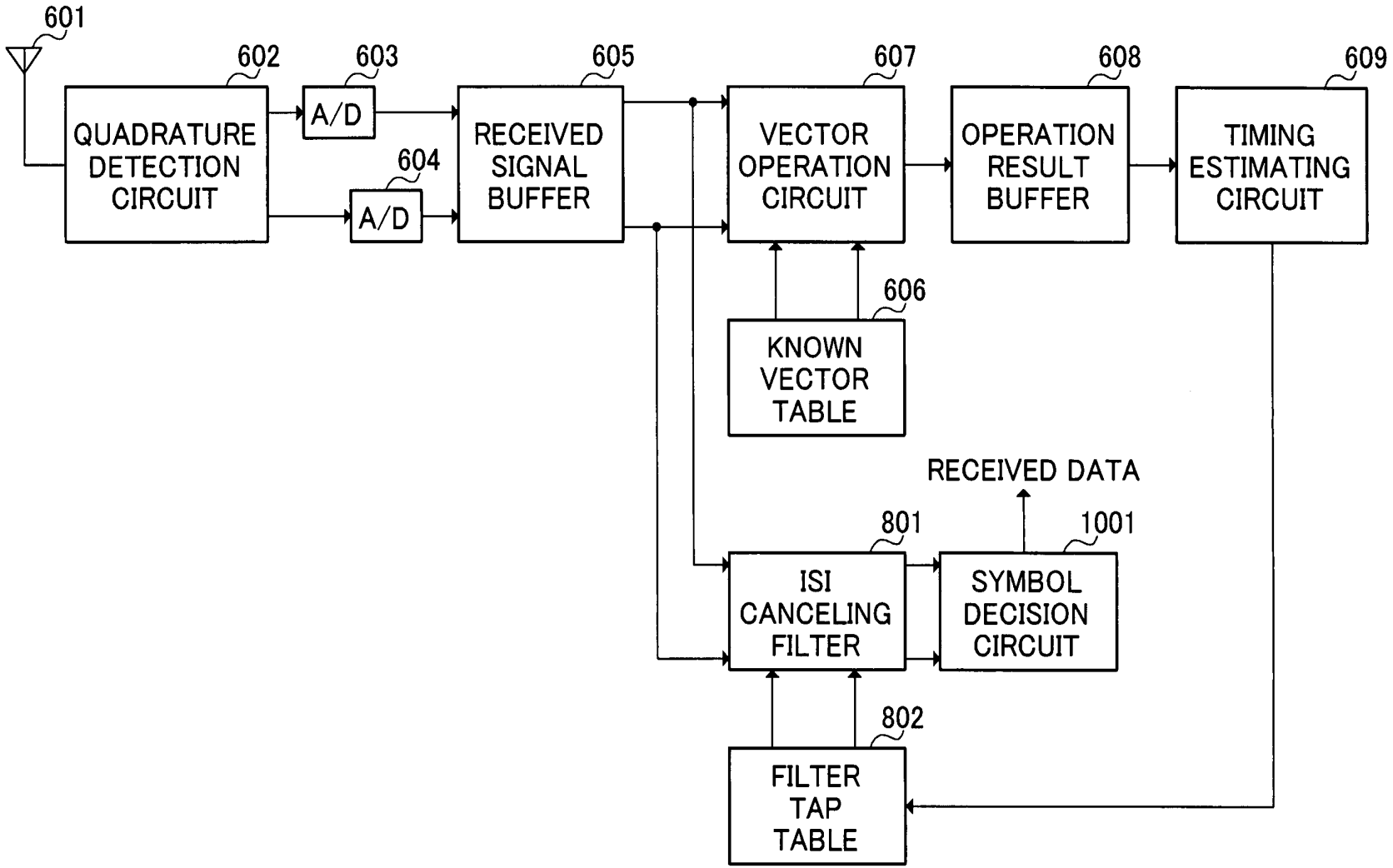
601
602
603
605
607
608
609
QUADRATURE DETECTION CIRCUIT
A/D
A/D
604
RECEIVED SIGNAL BUFFER
VECTOR OPERATION CIRCUIT
OPERATION RESULT BUFFER
TIMING ESTIMATING CIRCUIT
606
KNOWN VECTOR TABLE
RECEIVED DATA
801
1001
ISI CANCELING FILTER
SYMBOL DECISION CIRCUIT
802
FILTER TAP TABLE

FIG.15